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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/358,388 | 07/21/99 | UMEZAWA | K 0039-79292-2 |

| EXAMINER | |
|---|---|
| ART UNIT | PAPER NUMBER |
| 2814 | |

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**DATE MAILED:** 02/13/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/358,388 | UMEZAWA ET AL. | |
| | Examiner | Art Unit | |
| | Anh D. Mai | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-11 and 14-29* is/are pending in the application.

4a) Of the above claim(s) *16-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11,14,15 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *24 November 2000* is: a)☒ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

## DETAILED ACTION

### *Continued Prosecution Application*

1. The request filed on November 20, 2000 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/358,388 is acceptable and a CPA has been established. An action on the CPA follows.

### *Drawings*

2. The corrected or substitute drawings were received on November 20, 2000. The drawing is acceptable.

### *Response to Amendment*

3. The amendment filed October 19, 2000 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "at a substrate temperature *which is greater than* 1100°C *but less than or equal* to 1350°C" in claims 9 and 25-29.

Applicant is required to cancel the new matter in the reply to this Office Action.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 9-11, 14, 15 and 24-29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The original disclosure fails to provide support for: "at a substrate temperature *which is greater than* 1100°C *but less than or equal* to 1350°C".

Even though the temperature range disclosed in the specification is 1100°C to 1350°C, however, the insertion of "*greater than* , *but less than or equal"* is clearly new matters.

As best understood by examiner, the temperature range 1100°C to 1350°C is considered to be "greater than or equal to 1100°C but less than or equal to 1350°C".

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9, 11, 14, 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bose et al. (U.S. Patent No. 5,492,858).

As best understood by examiner, Bose '858 teaches a method of manufacturing a semiconductor substrate (10) having shallow trench isolation regions and device regions (32) sandwiched by the shallow trench isolation regions as claimed including:

(a) a first step of forming a plurality of grooves (20) on part of a surface of the semiconductor substrate (10);

(b) a second step of depositing oxide films (14) in the grooves by an organic silicon based CVD method and then removing upper parts of the oxide films so as to planarize a surface of a resultant structure, each of the active areas (32) of the semiconductor substrate serving as surface of a corresponding device region; and

(c) a third step of annealing the oxide films at a substrate temperature of about 1100°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Fig. 1-5, col. 4, l. 40-col. 6, l. 5).

Thus, Bose is shown to teach all of the features of the claim with the exception of planarize the deposited oxide film (14) until the surface areas of the semiconductor substrate are substantially exposed.

However, it is well known in the art to expose the active area after the formation of the isolation structure so that active device can be built.

Further, the annealing temperature of Bose is *about* 1100 °C. This temperature overlaps the claimed range. Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum annealing temperature for the oxide layer. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

Furthermore, since the annealing temperature of Bose overlaps the claimed range, therefore, the limitation of "dislocation density generated in the corresponding device region in

a vicinity of the grooves is less than $1/\mu m^2$" is an inherent result the annealing of the substrate at high temperature.

With respect to claim 11, the ambient during the anneal of Bose includes nitrogen gas.

With respect to claim 14, trench (20) of Bose has a depth (d) to width (l) ratio of less than 10.

With respect to claims 15 and 24, the arrangement of the grooves on the semiconductor substrate is clearly a design choice. The method of forming the STI is disclosed.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bose '858 as applied to claim 9 above, and further in view of Wolf et al. "Silicon Processing".

Bose is shown to teach all of the features of the claim with the exception of the method for depositing the conformal organic silicon based oxide film (14).

However, Wolf teaches an organic oxide film can be deposited by LPCVD to form a conformal layer. (page 194).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the organic based oxide film (14) of Bose by LPCVD as taught by Wolf to form a conformal layer.

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bose '858.

As best understood by examiner, Bose '858 teaches a method of manufacturing a semiconductor substrate (10) having shallow trench isolation regions and device regions (32) sandwiched by the shallow trench isolation regions as claimed including:

(a) forming a plurality of grooves (20) on part of a surface of the semiconductor substrate (10);

(b) depositing oxide films (14) in the grooves by an organic silicon based CVD method;

(c) annealing the oxide films at a substrate temperature of about 1100°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized; and

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure, each of the active areas (32) of the semiconductor substrate serving as top surface of a corresponding device region. (See Fig. 1-5, col. 4, l. 40-col. 6, l. 5).

Thus, Bose is shown to teach all of the features of the claim with the exception of planarize the deposited oxide film (14) until the surface areas of the semiconductor substrate are substantially exposed.

However, it is well known in the art to expose the active area after the formation of the isolation structure so that active device can be built.

Further, the annealing temperature of Bose is about 1100°C. This temperature overlaps the claimed range. Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum annealing temperature for the oxide layer. See In re Aller,

Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

Furthermore, since the annealing temperature of Bose overlaps the claimed range, therefore, the limitation of "dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^2$" is an inherent result the annealing of the substrate at high temperature.

8. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bose '858.

As best understood by examiner, Bose '858 teaches a method of manufacturing a semiconductor substrate (10) having shallow trench isolation regions and device regions (32) sandwiched by the shallow trench isolation regions as claimed including:

(a) forming a plurality of grooves (20) on part of a surface of the semiconductor substrate (10);

(b) burying oxide films (14) in the grooves by an organic silicon based CVD method;

(c) annealing the oxide films at a substrate temperature of about 1100°C so that the etching rate of the oxide is substantially identical to that of thermal oxide film. (See Fig. 1-5, col. 4, l. 40-col. 6, l. 5).

The annealing temperature of Bose is about 1100°C. This temperature overlaps the claimed range. Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum annealing temperature for the oxide layer. See In re Aller,

Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

Furthermore, since the annealing temperature of Bose overlaps the claimed range, therefore, the limitation of "higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates" as well as "Raman intensity corresponding to respective ring structures" are inherent result the *annealing of the substrate at high temperature*.

9. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bose '858.

As best understood by examiner, Bose '858 teaches a method of manufacturing a semiconductor substrate (10) having shallow trench isolation regions and device regions (32) sandwiched by the shallow trench isolation regions as claimed including:

(a) forming a plurality of grooves (20) on part of a surface of the semiconductor substrate (10);

(b) forming a thin thermal oxidation film (13) as part of inner walls of the grooves;

(c) depositing oxide films (14) directly on the thin thermal oxidation film by an organic silicon based CVD method;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure, each of the active areas (32) of the semiconductor substrate serving as top surface of a corresponding device region; and

(e) annealing the oxide films at a substrate temperature of about 1100°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Fig. 1-5, col. 4, l. 40-col. 6, l. 5).

Thus, Bose is shown to teach all of the features of the claim with the exception of planarize the deposited oxide film (14) until the surface areas of the semiconductor substrate are substantially exposed.

However, it is well known in the art to expose the active area after the formation of the isolation structure so that active device can be built.

Further, the annealing temperature of Bose is about 1100°C. This temperature overlaps the claimed range. Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum annealing temperature for the oxide layer. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

Furthermore, since the annealing temperature of Bose overlaps the claimed range, therefore, the limitation of "dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^{2}$" is an inherent result the annealing of the substrate at high temperature.

***Response to Arguments***

10. Applicant's arguments filed October 19, 2000 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 9-11, 14, 15 and 24-29 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
February 1, 2001

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